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| 09/708,450 | 11/09/2000 | YOSHITAKA NAKAMURA | 501.39149X00 | 2432 |

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| EXAMINER |
|---|
| OWENS, DOUGLAS W |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/708,450 | NAKAMURA ET AL. | |
| | Examiner | Art Unit | |
| | Douglas W Owens | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30 and 32-34* is/are pending in the application.

4a) Of the above claim(s) *1-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Claim 27 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 34 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 34 recites the limitation, "...wherein said first metal layer comprises a third metal layer...." The scope of the claim is vague because it is not known it the first metal layer is the same as the third metal layer or the first metal layer comprises several metal layers, the third layer being one of them.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20, 21 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,837,578 to Fan et al. in view of US patent No. 6,316,802 to Schindler et al.

Regarding claim 20, Fan et al. teaches a method of manufacturing an integrated circuit, comprising the steps of:

forming a C.O.B. structure (Col. 3, lines 20-23), which would have inherently required forming bit lines and contacts in a first insulating film;

forming a second interlayer insulating film (33) and electrode-forming insulating film (36);

etching holes in the electrode-forming insulating film (Fig. 3(e));

forming a conductive film (39) in the holes, and removing the electrode-forming insulating film to form cylindrical capacitor first electrodes (Fig. 3(h));

depositing a ferroelectric capacitor dielectric film (310) over the first electrodes; and

depositing and patterning a first a conductor layer (311) to form a second electrode.

Fan et al. does not teach forming a metal or metal compound for forming the lower electrode. Fan et al. does not teach patterning first and second conductor layers to form second electrodes, wherein the second conductor layer is tungsten. Fan et al. does not teach depositing a third interlayer insulating film to cover the second electrodes, and forming connection holes reaching the second electrodes and the first layer wiring.

Schindler et al. teaches using a metal to form the lower electrode (21) of a ferroelectric capacitor, patterning first (23a) and second (23b) conductor layers to form second electrodes and forming a third insulating film (25) and forming a connection hole to the second electrode and first wiring layer.

It would have been obvious to one of ordinary skill in the art to incorporate the platinum electrode used by Schindler et al. into the method of making an integrated circuit taught by Fan et al. since platinum is desirable for use as electrode material in ferroelectric capacitors due to the resistance it has to oxidation. If an oxide forms on the electrode layer, it would result in a low-k dielectric forming between the ferroelectric layer and the electrode and a reduction of capacitance. Schindler et al. teaches the additional advantage of forming a tungsten second conductor layer. It would have been obvious to incorporate this feature into the method taught by Fan et al. since it is desirable to avoid shifting of the hysteresis loop (Schindler et al., Col. 2, lines 66-67), as well as producing an electrode with low resistivity. It is also desirable to form a connection to the capacitor to give it functionality in the integrated circuit. Since etching is a well known method of forming contact holes in insulation film, it would have been obvious design choice to employ this known method of forming contacts. Schindler et al. further teaches contact holes to the second electrode and the wiring layer. It would have been obvious to incorporate the teaching of the first and second contact holes since it is desirable to enable communication between the capacitor and active devices.

Regarding claim 21, Fan et al. does not teach using the second layer of the second electrode as a mask to form the first layer of the second electrode after the

second layer is etched. Schindler et al. teaches a method wherein the second electrode is formed in layers. Since the tungsten layer is formed directly on top of the first conductive layer, it would have to be etched before etching the platinum layer. It would have been obvious to incorporate the teaching of Schindler et al. into the method taught by Fan et al. for reasons discussed above.

Regarding claims 26 and 27, Fan et al. teaches a method of making an integrated circuit, comprising the steps of:

forming first electrodes on a first insulating film;

forming a capacitor dielectric film over the first electrode; and

forming continuous second electrodes over the capacitor dielectric film.

Fan et al. does not teach a method wherein the formation of the second electrode includes forming a first metal layer. Fan et al. does not teach a second metal layer having a greater thickness and lower resistivity than the first metal layer. Schindler et al teaches a method, wherein the second electrode comprises a first and second metal layer, the second metal layer have a greater thickness and lower resistivity than the first metal layer (Col. 4, lines 43-44; Col. 1, lines 58-60; Col. 3, lines 5-7). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Schindler et al. into the teaching of Fan et al. for reasons discussed above.

Regarding claim 28, Fan et al. does not teach a method of producing a semiconductor device, wherein the first metal layer is platinum or ruthenium and the second metal layer is tungsten or tungsten nitride. Schindler et al teaches a method, wherein the first metal layer is platinum and the second metal layer is tungsten. It would

have been obvious to one of ordinary skill to incorporate the teaching of Schindler et al. into the method taught by Fan et al. for reasons discussed above.

6. Claims 22-25 and 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. in view of US patent No. 5,854,104 to Onishi et al.

Regarding claim 22, Fan et al. teaches a method of making an integrated circuit, comprising the steps of:

forming first electrodes on a first insulating film;

forming a capacitor dielectric film over the first electrode; and

forming second electrodes over the capacitor dielectric film.

Fan et al. does not teach forming a second insulating film over the second electrodes, wherein the film has an opening for exposing a part of the second electrodes. Fan et al. does not teach a method wherein the formation of the second electrode includes forming a first metal layer by CVD. Fan et al. does not teach a method wherein the formation of the second electrode includes forming a second metal layer not containing oxygen over the first metal layer.

Onishi et al. teaches forming a second insulating film over the second electrode having an opening for exposing a part of the second electrodes. Onishi et al. teaches a method wherein forming the second electrode includes depositing a platinum layer by a known method (Col. 5, lines 12 and 13). Onishi et al. teaches a method wherein the formation of the second electrode includes forming a second metal layer not containing oxygen over and directly contacting the first metal layer. It would have been obvious to one of ordinary skill in the art to form the opening in the second insulating film since it is

desirable to form a connection to the capacitor to give it functionality in the integrated circuit. It would have further been obvious to provide a conductor layer in the opening since it is needed to provide a connection. It would have been obvious to use CVD to deposit the metal since it is a known method, as suggested by Onishi et al. It would have been further obvious to incorporate the method taught by Onishi et al. into the method taught by Fan et al. for reasons discussed above.

Regarding claim 23, Fan et al. does not teach a method of making an integrated circuit, wherein the first metal layer is platinum or ruthenium. Onishi et al. teaches using platinum for the first metal layer (13) of a ferroelectric capacitor. It would have been obvious to one of ordinary skill in the art to incorporate the platinum electrode used by Onishi et al. into the method of making an integrated circuit taught by Fan et al. since platinum is desirable for use as electrode material in ferroelectric capacitors due to the resistance it has to oxidation.

Regarding claims 24 and 33, Fan et al. does not teach a method, wherein the second metal layer comprises tungsten or tungsten nitride. Onishi et al. teaches a method, wherein the second metal layer comprises titanium nitride. It would have been obvious to one of ordinary skill in the art to substitute titanium nitride with tungsten nitride since the two refractory metals have similar properties.

Regarding claims 25 and 30, Fan et al. does not teach a method of making an integrated circuit, wherein the second metal layer is formed by sputtering. Onishi et al. teaches a method of making an integrated circuit, wherein the second metal layer is

formed by sputtering (Col. 5, lines 9-14). It would have been obvious to incorporate the teaching of Onishi et al. into the teaching of Fan et al. for reasons discussed above.

Regarding claim 29, Fan et al. teaches a method of making an integrated circuit, including the steps of:

forming a first electrode over a first insulating film;

forming a capacitor dielectric over the first electrode; and

forming a second electrode over the capacitor dielectric.

Fan et al. does not teach a method of making an integrated circuit, wherein the formation step of the second electrode includes forming a first metal layer and a second metal layer. Onishi et al. teaches a method of making an integrated circuit, wherein the formation step of the second electrode includes forming a first metal layer and a second metal layer. It would have been obvious incorporate the teaching of Onishi et al. into the method taught by Fan et al. for reasons discussed above.

***Response to Arguments***

7. Applicant's arguments with respect to claims 20, 21 and 26-28 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed August 15, 2002 have been fully considered but they are not persuasive.

The applicant argues, with respect to the rejection independent claim 22, Onishi does teach a method wherein the formation of the second electrode includes forming a second metal not containing oxygen over the first metal layer, with the first and second layers being directly connecting. Onishi teaches a method of forming these layers in lines 18-63 of column 4. Moreover, Onishi teaches a method, wherein the cited materials are employed. Capacitor electrodes are routinely formed in the VLSI fabrication and the technique by which an upper electrode would be formed only involves ordinary skill in the art.

The applicant argues that Onishi does not suggest that the first metal film is provided within spaces between first electrodes because Onishi only shows only one capacitor, which is understood by the applicant to mean that only one capacitor is made. The method taught by Onishi would have included more than one transistor and one capacitor since it is made for use in a nonvolatile random access memory device (Col. 1, lines 8-14), which cannot be manufactured using only one transistor and one capacitor.

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DWO
November 18, 2002